11.4.9 Memory

The Main Board has six types of memory:

- **DRAM** provides memory for graphics, sound and other software requirements.
- **DRAM Emulator**.
- **EPROM** contains the game software.
- **SRAM** provides memory for metering.
- **EEPROM** contains high reliability configuration data.
- The Real Time Clock also contains a number of bytes of SRAM.

DRAM

The Main Board has 2 Mbyte of dynamic RAM as standard. The ARM250 can address a **maximum** of 4 Mbytes of DRAM, using its built in DRAM controller. The ARM250 directly drives the multiplexed address lines (`RA[9:0]`), row and column (`RAS`, `CAS[3:0]`) strobes, output (`OE[1:0]`), and write enable (`WE[1:0]`) signals.

The Main Board must have at least 1 Mbyte of dynamic RAM fitted, with the other 1 Mbyte being optional. Using 4 Mbit DRAMs the maximum possible (in 4 devices) is 2 Mbytes. The first bank of DRAMs is dual pitched to allow the use of 16 Mbit DRAMs allowing 4 Mbytes to be fitted in only 2 chips. As this is the maximum addressable, the second bank would not be fitted.

DRAM Emulator

The DRAM emulator logic detects an access to the interrupt vector table and substitutes either ROM or a fixed branch instruction (to EPROM) in place of the DRAM.

EPROM

The data bus for EPROMs is 32 bit wide. The Main Board contains sockets for 8 EPROMs, which can be configured to 1, 2, or 4 Mbit chips and each is 16 bit wide. This allows a maximum of 4 Mbytes of EPROMs, which is also the ARM250 addressing limit.

To expand the memory beyond 4 Mbytes, the on-board EPROMs can be replaced by an external memory PCB which sits onto the main board

Meters SRAM

The Main Board provides 32 kbytes of Static Random Access Memory (SRAM) with battery back-up for the electronic meters.

The SRAM contains machine metering information, such as money in/out, game history, etc. It is critical that this data is preserved reliably, and various jurisdictions require multiple backups of the data.

Three standard low power SRAMs are fitted to the board. The data is usually replicated three times, so that each chip contains identical data. Each memory is checked against the other to verify that the stored data is correct.

Each chip is mapped to the same address, and the chip selected depends on the bank select register. Access is mutually exclusive, increasing security with only one chip visible in the CPU address space at a time. If the CPU crashes and